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EXAMINER	
MILORD, MARCEAU	

ART UNIT	PAPER NUMBER
2682	8

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/691,634	MOLOUDI ET AL.	
	Examiner	Art Unit	
	Marceau Milord	2682	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 October 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-95* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-95* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 October 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *6* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-18, 20-38, 40-59, 61-94 are rejected under 35 U.S.C. 102(e) as being anticipated by Chen (US Patent No 6194962 B1)

Regarding claim 1, Chen discloses an amplifier (figs. 3-4), comprising: a plurality of differential pairs (MP1 and MP2) coupled together through a common differential output, each differential pair (MP1 and MP2) having a current control input (col. 2, lines 41-61; col. 3, lines 38-57; col. 5, lines 3-32); and a current switch (32 of fig. 3) coupled to the current control input of one of the differential pairs to selectively switch said one of the differential pairs in or out of the amplifier (col. 3, line 58- col. 4, line 67; col. 6, line 45- col. 7, line 22).

Regarding claim 2, Chen discloses an amplifier (figs. 3-4), wherein the differential pairs each comprises first and second transistors coupled together through a common node, the common node comprising the current control input (col. 3, lines 39-67; col. 4, line 65- col. 5, line 45).

Regarding claim 3, Chen discloses an amplifier (figs. 3-4), wherein the transistors (MP1 and MP2 or MP 3 and MP 4 of fig. 4) each comprises a field effect transistor (col. 3, lines 54-67; col. 7, lines 1-27).

Regarding claim 4, Chen discloses an amplifier (figs. 3-4), wherein the first and second transistors (MP1 and MP2 or MP 3 and MP 4 of fig. 4) in each differential pair each comprises a source coupled to its respective common node (col. 4, line 65- col. 5, line 64).

Regarding claim 5, Chen discloses an amplifier (figs. 3-4), wherein the first and second transistors (MP1 and MP2 or MP 3 and MP 4 of fig. 4) in each of the differential pairs each comprises a gate, the gates of the first transistors being coupled together and the gates of the second transistors being coupled together to form a differential input (col. 5, lines 3- 42; col. 6, lines 1-31).

Regarding claim 6, Chen discloses an amplifier (figs. 3-4), wherein the first and second transistors (MP1 and MP2 or MP 3 and MP 4 of fig. 4) in each of the differential pairs each comprises a drain, the drains of the first transistors being coupled together and the drains of the second transistors being coupled together to form the differential output (col. 5, lines 3-45; col. 6, lines 1-31).

Regarding claim 7, Chen discloses an amplifier (figs. 3-4), wherein the current switch (32 of fig. 3) comprises a transistor (MP1 of fig. 3; col 5, lines 1- 37).

Regarding claim 8, Chen discloses an amplifier (figs. 3-4), wherein the transistor comprises a field effect transistor (col. 3, lines 54-67; col. 7, lines 1-27).

Regarding claim 9, Chen discloses an amplifier (figs. 3-4), wherein the transistor comprises a drain coupled to its respective current control input (col. 5, lines 3-37; col. 6, lines 1-56).

Regarding claim 10, Chen discloses an amplifier (figs. 3-4), wherein the current switch (32 of fig. 3) comprises a current source (30 of fig. 3) having a switch control input (32 of fig. 3; col. 4, lines 45-67; col. 5, lines 3- 45).

Regarding claim 11, Chen discloses an amplifier (figs. 3-4), further comprising a bias circuit coupled to the switch control input (col. 3, line 47- col. 4, line 19).

Regarding claim 12, Chen discloses an amplifier (figs. 3-4), wherein the bias circuit generates a bias current which is substantially independent of temperature, the bias current being applied to the switch control input (col. 3, line 47- col. 4, line 19).

Regarding claim 13, Chen discloses an amplifier (figs. 3-4), wherein the bias circuit comprises a first bias circuit having a first bias current exhibiting a positive temperature coefficient, a second bias circuit having a second bias current exhibiting a negative temperature coefficient, and a summer to sum the first and second bias currents, the summed first and second bias currents being applied to the switch control input (col. 4, lines 3-67; col. 5, lines 3- 45; col. 7, lines 23- 67).

Regarding claim 14, Chen discloses an amplifier (figs. 3-4), wherein the summer comprises a cascode current mirror (col. 5, lines 1-15; col. 7, lines 1- 33).

Regarding claim 15, Chen discloses an amplifier (figs. 3-4), wherein the current source comprises a field effect transistor having a gate comprising the switch control input (col. 3, lines 54-67; col. 5, lines 3-37).

Regarding claim 16, Chen discloses an amplifier (figs. 3-4), further comprising a matching circuit coupled to the common differential output (col. 3, line 47- col. 4, line 32).

Regarding claim 17, Chen discloses an amplifier (figs. 3-4), wherein the matching circuit converts a differential current from the common differential output to a single-ended current (col. 3, line 47- col. 4, line 48).

Regarding claim 18, Chen discloses an amplifier (figs. 3-4), wherein the matching circuit provides an impedance transformation which is independent of whether said one of the differential pairs is switched in or out of the amplifier (col. 5, lines 3-37; col. 7, lines 1-46).

19. The amplifier of claim 16 wherein the common differential output comprises first and second outputs, and the matching circuit comprises an inductor having a first end coupled to the first output and a capacitor having a first end coupled to the second output, the inductor and capacitor each having second end coupled together.

Regarding claim 20, Chen discloses an amplifier (figs. 3-4), wherein the differential pairs are further coupled together through a common differential input, the amplifier further comprising an input stage coupled to the common differential input (col. 5, lines 3- 42; col. 6, lines 1-31).

Regarding claim 21, Chen discloses an amplifier (figs. 3-4), further comprising a plurality of current switches each coupled to the current control input for a different one of the differential pairs to selectively switch its respective differential pair in or out of the amplifier (col. 5, lines 3-37; col. 7, lines 1-46).

Regarding claim 22, Chen discloses an amplifier (figs. 3-4), comprising: a plurality of amplifying stages each having first and second transistors (MP1 and MP2 of fig. 3), the first and

second transistors (MP1 and MP2 of fig. 3), each having first, second and third nodes, the first nodes of the first transistors being coupled together and the first nodes of the second transistors being coupled together to form a differential output, the second nodes of the first transistors being coupled together and the second nodes of the second transistors being coupled together to form a differential input, and the third node of each of the first transistors being coupled to the third node of its respective second transistor to form a current control input for each of the amplifying stages (col. 2, lines 41-61; col. 3, lines 38-57; col. 5, lines 3-32); and a current switch coupled to the current control input of one the amplifying stage to switch said one of the amplifying stages in or out of the amplifier (col. 3, line 58- col. 4, line 67; col. 6, line 45- col. 7, line 22).

Regarding claim 23, Chen discloses an amplifier (figs. 3-4), wherein the transistors each comprise a field effect transistor (col. 3, lines 54-67; col. 7, lines 1-27).

Regarding claim 24, Chen discloses an amplifier (figs. 3-4), wherein the third nodes each comprise a source (col. 4, line 65- col. 5, line 64).

Regarding claim 25, Chen discloses an amplifier (figs. 3-4), wherein the second nodes each comprise a gate (col. 5, lines 3- 42).

Regarding claim 26, Chen discloses an amplifier (figs. 3-4), wherein the first nodes each comprise a drain (col. 5, lines 3-37).

Regarding claim 27, Chen discloses an amplifier (figs. 3-4), wherein the current switch comprises a transistor (MP1 of fig. 3; col 5, lines 1- 37).

Regarding claim 28, Chen discloses an amplifier (figs. 3-4), wherein the transistor comprises a field effect transistor (col. 3, lines 54-67; col. 7, lines 1-27).

Regarding claim 29, Chen discloses an amplifier (figs. 3-4), wherein the transistor comprises a drain coupled to its respective current control input (col. 5, lines 3-37; col. 6, lines 1-56).

Regarding claim 30, Chen discloses an amplifier (figs. 3-4), wherein the current switch comprises a current source having a switch control input (32 of fig. 3; col. 4, lines 45-67; col. 5, lines 3- 45).

Regarding claim 31, Chen discloses an amplifier (figs. 3-4), comprising a bias circuit coupled to the switch control input (col. 3, line 47- col. 4, line 19).

Regarding claim 32, Chen discloses an amplifier (figs. 3-4), wherein the bias circuit generates a bias current, which is substantially independent of temperature; the bias current being applied the switch control input (col. 3, line 47- col. 4, line 19).

Regarding claim 33, Chen discloses an amplifier (figs. 3-4), wherein the bias circuit comprises a first bias circuit having a first bias current exhibiting a positive temperature coefficient, a second bias circuit having a second bias current exhibiting a negative temperature coefficient, and a summer to sum the first and second bias currents, the summed first and second bias currents being applied to the switch control input (col. 4, lines 3-67; col. 5, lines 3- 45; col. 7, lines 23- 67).

Regarding claim 34, Chen discloses an amplifier (figs. 3-4), wherein the summer comprises a cascode current mirror (col. 5, lines 1-15; col. 7, lines 1- 33).

Regarding claim 35, Chen discloses an amplifier (figs. 3-4), wherein the current source comprises a field effect transistor having a gate comprising the switch control input (col. 3, lines 54-67; col. 5, lines 3-37).

Regarding claim 36, Chen discloses an amplifier (figs. 3-4), further comprising a matching circuit coupled to the differential output (col. 3, line 47- col. 4, line 32).

Regarding claim 37, Chen discloses an amplifier (figs. 3-4), wherein the matching circuit converts a differential current from the differential output to a single-ended current (col. 3, line 47- col. 4, line 48).

Regarding claim 38, Chen discloses an amplifier (figs. 3-4), wherein the matching circuit provides an impedance transformation which is independent of whether said one of the amplifying stages is switched in or out of the circuit (col. 5, lines 3-37; col. 7, lines 1-46).

Regarding claim 40, Chen discloses an amplifier (figs. 3-4), further comprising an input stage coupled to the differential input (col. 5, lines 3- 42).

Regarding claim 41, Chen discloses an amplifier (figs. 3-4), further comprising a plurality of current switches each coupled the current control input for a different one of the amplifying stages to selectively switch its respective amplifying stage in or out of the amplifier (col. 5, lines 3-37; col. 7, lines 1-46).

Regarding claim 42, Chen discloses an amplifier (figs. 3-4), comprising:
a plurality of amplifying stages coupled together, each of the amplifying stages having a current control input (col. 2, lines 41-61; col. 3, lines 38-57; col. 5, lines 3-32); and a current switch coupled to the current control input of one of the amplifying stages to selectively switch said one of the amplifying stages in or out of the circuit (col. 3, line 58- col. 4, line 67; col. 6, line 45- col. 7, line 22).

Regarding claim 43, Chen discloses an amplifier (figs. 3-4), wherein the amplifying stages each comprises first and second transistors coupled together through a common node, the

common node comprising the current control input (col. 3, lines 39-67; col. 4, line 65- col. 5, line 45).

Regarding claim 44, Chen discloses an amplifier (figs. 3-4), wherein the transistors each comprise a field effect transistor (col. 3, lines 54-67; col. 7, lines 1-27).

Regarding claim 45, Chen discloses an amplifier (figs. 3-4), wherein the first and second transistors (MP1 and MP2 or MP 3 and MP 4 of fig. 4) in each amplifying stage comprises a source coupled to its respective common node (col. 4, line 65- col. 5, line 64).

Regarding claim 46, Chen discloses an amplifier (figs. 3-4), wherein the first and second transistors (MP1 and MP2 or MP 3 and MP 4 of fig. 4) in each of the amplifying stages each comprises a gate, the gates of the first transistors being coupled together and the gates of the second transistors being coupled together to form a differential input (col. 4, line 65- col. 5, line 64).

Regarding claim 47, Chen discloses an amplifier (figs. 3-4), wherein the first and second transistors (MP1 and MP2 or MP 3 and MP 4 of fig. 4) in each of the differential pairs each comprises a drain, the drains of the first transistors being coupled together and the drains of the second transistors being coupled together to form a differential output (col. 5, lines 3-45; col. 6, lines 1-31).

Regarding claim 48, Chen discloses an amplifier (figs. 3-4), wherein the current switch comprises a transistor (col. 3, lines 54-67; col. 7, lines 1-27).

Regarding claim 49, Chen discloses an amplifier (figs. 3-4), wherein the transistor comprises a field effect transistor (col. 3, lines 54-67; col. 7, lines 1-27).

Regarding claim 50, Chen discloses an amplifier (figs. 3-4), wherein the transistor comprises a drain coupled to its respective current control input (col. 5, lines 3-37; col. 6, lines 1-56).

Regarding claim 51, Chen discloses an amplifier (figs. 3-4), wherein the current switch comprises a current source having a switch control input (32 of fig. 3; col. 4, lines 45-67; col. 5, lines 3- 45).

Regarding claim 52, Chen discloses an amplifier (figs. 3-4), further comprising a bias circuit coupled to the switch control inputs (col. 3, line 47- col. 4, line 19).

Regarding claim 53, Chen discloses an amplifier (figs. 3-4), wherein the bias circuit generates a bias current which is substantially independent of temperature, the bias current being applied to the switch control input (col. 3, line 47- col. 4, line 19).

Regarding claim 54, Chen discloses an amplifier (figs. 3-4), wherein the bias circuit comprises a first bias circuit having a first bias current exhibiting a positive temperature coefficient, a second bias circuit having a second bias current exhibiting a negative temperature coefficient, and a summer to sum the first and second bias currents, the summed first and second bias currents being applied to the switch control input (col. 4, lines 3-67; col. 5, lines 3- 45; col. 7, lines 23- 67).

Regarding claim 55, Chen discloses an amplifier (figs. 3-4), wherein the summer comprises a cascode current mirror (col. 3, lines 54-67; col. 5, lines 3-37).

Regarding claim 56, Chen discloses an amplifier (figs. 3-4), wherein the current source comprises a field effect transistor having a gate comprising the switch control input (col. 3, lines 54-67; col. 5, lines 3-37).

Regarding claim 57, Chen discloses an amplifier (figs. 3-4), further comprising a matching circuit coupled to the differential output (col. 3, line 47- col. 4, line 32).

Regarding claim 58, Chen discloses an amplifier (figs. 3-4), wherein the matching circuit converts a differential current from the differential output to a single-ended current (col. 3, line 47- col. 4, line 48).

Regarding claim 59, Chen discloses an amplifier (figs. 3-4), wherein the matching circuit provides an impedance transformation which is independent of whether said one of the amplifying stages is switched in or out of the circuit (col. 5, lines 3-37; col. 7, lines 1-46).

Regarding claim 61, Chen discloses an amplifier (figs. 3-4), wherein the amplifying stages are coupled together to form a differential input, the amplifier further comprising an input stage coupled to the differential input (col. 5, lines 3- 42; col. 6, lines 1-31).

Regarding claim 62, Chen discloses an amplifier (figs. 3-4), further comprising a plurality of current switches each coupled to the current control input for a different one of the amplifying stages to selectively switch its respective amplifying stage in or out of the amplifier (col. 5, lines 3-37; col. 7, lines 1-46).

Regarding claim 63, Chen discloses an amplifier (figs. 3-4), comprising a digitally programmable power level and a matching circuit, which is substantially independent of the programmed power level (col. 2, lines 41-61; col. 3, lines 38-57; col. 5, lines 3-32).

Regarding claim 64, Chen discloses an amplifier (figs. 3-4), wherein the amplifier comprises CMOS (col. 6, lines 5-36).

Regarding claim 65, Chen discloses an amplifier (figs. 3-4), comprising a plurality of amplifying stages coupled together, each of the amplifying stages having a current control input,

and a plurality of current switches to digitally program the power level of the amplifier, the current switches each being coupled to the current control input for a different one of the amplifying stages to selectively switch its respective amplifying stage in or out of the amplifier (col. 5, lines 3-37; col. 7, lines 1-46).

Regarding claim 66, Chen discloses an amplifier (figs. 3-4), wherein the amplifying stages each comprises first and second transistors coupled together through a common a node, the common node comprising the current control input (col. 3, lines 39-67; col. 4, line 65- col. 5, line 45).

Regarding claim 67, Chen discloses an amplifier (figs. 3-4), wherein the transistors each comprise a field effect transistor (col. 3, lines 54-67; col. 7, lines 1-27).

Regarding claim 68, Chen discloses an amplifier (figs. 3-4); wherein the first and second transistors in each amplifying stage comprises a source coupled to its respective common node (col. 4, line 65- col. 5, line 64).

Regarding claim 69, Chen discloses an amplifier (figs. 3-4), wherein the first and second transistors in each of the amplifying stages each comprises a gate, the gates of the first transistors being coupled together and the gates of the second transistors being coupled together to form a differential input (col. 4, line 65- col. 5, line 64).

Regarding claim 70, Chen discloses an amplifier (figs. 3-4), wherein the first and second transistors in each of the differential pairs each comprises a drain, the drains of the first transistors being coupled together and the drains of the second transistors being coupled together to form a differential output (col. 5, lines 3-45; col. 6, lines 1-31).

Regarding claim 71, Chen discloses an amplifier (figs. 3-4), wherein the current switches each comprise a transistor (col. 3, lines 54-67; col. 7, lines 1-27).

Regarding claim 72, Chen discloses an amplifier (figs. 3-4), wherein the transistors each comprise a field effect transistor (col. 3, lines 54-67; col. 7, lines 1-27).

Regarding claim 73, Chen discloses an amplifier (figs. 3-4 wherein the transistors each comprises a drain coupled to its respective current control input (col. 5, lines 3-37; col. 6, lines 1-56).

Regarding claim 74, Chen discloses an amplifier (figs. 3-4), wherein the current switches each comprise a current source having a switch control input (32 of fig. 3; col. 4, lines 45-67; col. 5, lines 3- 45).

Regarding claim 75, Chen discloses an amplifier (figs. 3-4) comprising a plurality of bias circuits each coupled to a different one of the switch control inputs (col. 3, line 47- col. 4, line 19).

Regarding claim 76, Chen discloses an amplifier (figs. 3-4), wherein the bias circuits each generates a bias current which is substantially independent of temperature, the bias current being applied to its respective switch control input (col. 3, line 47- col. 4, line 19).

Regarding claim 77, Chen discloses an amplifier (figs. 3-4) wherein the bias circuits each comprises a first bias circuit having a first bias current exhibiting a positive temperature coefficient, a second bias circuit having a second bias current exhibiting a negative temperature coefficient, and a summer to sum the first and second bias currents, the summed first and second bias currents being applied to the its respective switch control input (col. 4, lines 3-67; col. 5, lines 3- 45; col. 7, lines 23- 67).

Regarding claim 78, Chen discloses an amplifier (figs. 3-4) wherein the summer comprises a cascode current mirror (col. 3, lines 54-67; col. 5, lines 3-37).

Regarding claim 79, Chen discloses an amplifier (figs. 3-4), wherein the current sources each comprises a field effect transistor having a gate comprising the switch control input (col. 3, lines 54-67; col. 5, lines 3-37).

Regarding claim 80, Chen discloses an amplifier (figs. 3-4), comprising:
a plurality of amplifying stages coupled together; switching means for switching one of the amplifying stages in or out of the amplifier to program power of the amplifier (col. 2, lines 41-61; col. 3, lines 38-57; col. 5, lines 3-32); and matching means for matching a load coupled to an output of the amplifier, the matching means being substantially independent of the programmed power (col. 6, line 45- col. 7, line 22).

Regarding claim 81, Chen discloses an amplifier (figs. 3-4), wherein each of said one of the amplifying stage comprises first and second transistors coupled together through a common a node, the common node comprising the current control input (col. 3, lines 39-67; col. 4, line 65- col. 5, line 45).

Regarding claim 82 Chen discloses an amplifier (figs. 3-4), wherein the transistors each comprises a field effect transistor (col. 3, lines 54-67; col. 7, lines 1-27).

Regarding claim 83, Chen discloses an amplifier (figs. 3-4), wherein the first and second transistors each comprises a source coupled to its respective common node (col. 4, line 65- col. 5, line 64).

Regarding claim 84, Chen discloses an amplifier (figs. 3-4), wherein the amplifying stages each comprises first and second field effect transistors each having a gate, the gates of the

first transistors being coupled together and the gates of the second transistors being coupled together to form a differential input (col. 4, line 65- col. 5, line 64).

Regarding claim 85, Chen discloses an amplifier (figs. 3-4), wherein the amplifying stages each comprises first and second field effect transistors each having a drain, the drains of the first transistors being coupled together and the drains of the second transistors being coupled together to form a differential output (col. 5, lines 3-45; col. 6, lines 1-31).

Regarding claim 86, Chen discloses an amplifier (figs. 3-4), wherein the switching means comprises a transistor (col. 3, lines 54-67; col. 7, lines 1-27).

Regarding claim 87, Chen discloses an amplifier (figs. 3-4), wherein the transistor comprises a field effect transistor (col. 3, lines 54-67; col. 7, lines 1-27).

Regarding claim 88, Chen discloses an amplifier (figs. 3-4), wherein the transistor comprises a drain coupled to said one of the amplifying stages (col. 5, lines 3-37; col. 6, lines 1-56).

Regarding claim 89, Chen discloses an amplifier (figs. 3-4), wherein the switching means comprises a current source having a switch control input (32 of fig. 3; col. 4, lines 45-67; col. 5, lines 3- 45).

Regarding claim 90, Chen discloses an amplifier (figs. 3-4), further comprising a bias circuit coupled to the switch control input (col. 3, line 47- col. 4, line 19).

Regarding claim 91, Chen discloses an amplifier (figs. 3-4), wherein the bias circuit comprises means for generating a bias current which is substantially independent of temperature, the bias current being applied to the switch control input (col. 3, line 47- col. 4, line 19).

Regarding claim 92, Chen discloses an amplifier (figs. 3-4), wherein the bias circuit comprises means for generating a first bias current exhibiting a positive temperature coefficient, means for generating a second bias current exhibiting a negative temperature coefficient, and means for summing the first and second bias currents, the summed first and second bias currents being applied to the switch control input (col. 4, lines 3-67; col. 5, lines 3- 45; col. 7, lines 23-67).

Regarding claim 93, Chen discloses an amplifier (figs. 3-4), wherein the summer comprises a cascode current mirror (col. 3, lines 54-67; col. 5, lines 3-37).

Regarding claim 94, Chen discloses an amplifier (figs. 3-4), wherein the matching means comprises means for converting a differential current generated by the amplifier stage to a single-ended current, the single ended current being coupled to the amplifier output (col. 3, line 47- col. 4, line 48).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 19, 39, 60, 95 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (US Patent No 6194962 B1) in view of Ciccarelli et al (US Patent No 6175279 B1).

Regarding claims 19, 39, 60, Chen discloses everything claimed as explained above except an inductor having a first end coupled to the first output and a capacitor having a first end

coupled to the second output, the inductor and capacitor each having second end coupled together.

However, Ciccarelli et al discloses an amplifier having an adjustable current source, which can be controlled to provide the requisite level of performance at reduced current consumption. The current source is then designed to provide adjustable bias current for the amplifier. Furthermore, Ciccarelli shows in figure 5A, a capacitor 1514 that connects to analog ground and the other end of inductor 1516 connects to one end of resistors 1518 and 1520 and the base of transistor 1540. Capacitor 1514 and inductor 1516 provide noise matching. Inductors 1516 and 1532 also provide matching of the LNA input and output, respectively. Inductor 1542 also provides degeneration of the emitter impedance to improve linearity (col. 4, line 35- col. 5, line 13; col. 9, line 25-col. 10, line 35). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Ciccarelli to the system of Chen in order to determine the performance of the amplifier, such as linearity and noise performance.

Claim 95 contains similar limitations addressed in claims 19, 39, 60, and therefore is rejected under a similar rationale.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Van Horn et al US Patent No 5867064 discloses a method and apparatus for improving intermodulation in a feed-forward amplifier.

Sirna et al US Patent No 6100759 discloses a low noise integrated differential AC amplifier, which includes a cascode differential input stage comprising first and second branches.

Younis et al US Patent No 6134430 discloses a programmable dynamic range receiver, which provides the requisite level of performance at reduced power consumption.

Devito et al USS Patent No 5418498 discloses a low jitter ring oscillators.

Kaufman et al US Patent No 6240142 B1 discloses a quadrature modulator and demodulator, which provide the requisite level of performance while minimizing power consumption.

Huijsing et al US Patent No 5734297 discloses a rail-to-rail input stage with constant gm and constant common-mode output currents.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marceau Milord whose telephone number is 703-306-3023. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vivian C. Chin can be reached on 703-308-6739. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9314.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

MARCEAU MILORD

Marceau Milord
Examiner
Art Unit 2682